§103 Rejection of the Claims

Claims 1-11, 13-17, and 19-23 were rejected under 35 USC § 103(a) as being unpatentable over Horiguchi et al. ("Direct Tunneling Memory - - DTM Utilizing..."). The Examiner asserts that Horiguchi includes edge defined gate structures as required by Applicants' independent claims 1, 7, and 14. However, Applicants assert that Horiguchi does not disclose or teach, either expressly or inherently, an edged defined vertical floating gate, as is required by each of the unamended independent claims 1, 7, and 14. Correspondingly, this rejection is not sustainable with respect to independent claims 1, 7, and 14.

The Examiner asserts that the sidewall described in Horiguchi is equivalent to the Applicants' unamended claim requirements corresponding to an edge defined vertical floating gate. Yet, Horiguchi specifically states that the sidewall acts as a control gate, and not as a floating gate. (Horiguchi, pg. 11.6.1, col. 2, para. 1; Fig. 2) Accordingly, Horiguchi fails to teach or disclose, either expressly or inherently, each and every unamended claim requirement embodied in Applicants' unamended independent claims 1, 7, and 14. Thus, the rejections should be withdrawn.

Moreover, Applicants' amended independent claims 1, 7, and 14 require edge defined gates having sub lithographic dimensions and Horiguchi fails to produce, disclose, or teach edge defined gates having the required sub lithographic dimensions. As has been previously asserted by the Applicant, Horiguchi uses standard lithography for production of gate structures. Therefore, Horiguchi is incapable of producing edge defined gates having sub lithographic dimensions. Regardless of the process used in Horiguchi, the gates produced in Horiguchi are not of sub lithographic dimensions, which is required by each of the Applicants' amended independent claims 1, 7, and 14.

Furthermore, as one or ordinary skill in the art will appreciate edge-defined MOS technology ("EDMOS") permits sub lithographic dimensions of gate lengths and widths unlike standard lithographically defined geometrics. This is so, because EDMOS technology uses the thickness of the deposited films in determining gate lengths and widths. Horiguchi is directed toward suppressing gate leakage and improving retention time during high speed write/erase operations wherein low voltage is achieved. But, Horiguchi does not teach or disclose, either expressly or inherently, edge defined gates having sub lithographic dimensions as is required by Applicants' amended independent claims 1, 7, and 14. Correspondingly, the present rejections

are not sustainable.

Additionally, 2-6, 8-11, 13-17, and 19-23 are dependent claims derived from the rejected independent claims 1, 7, and 14. Thus, the rejections of these claims are no longer sustainable, and the Applicants respectfully request that these rejections also be withdrawn.

Claims 1-23 were rejected under 35 USC § 103(a) as being unpatentable over Horiguchi et al. ("Direct Tunneling Memory (DTM Utilizing...") in view of Watanabe (U.S. Patent No. 6,133,601) or Hong et al. (U.S. Patent No. 5,625,213).

As previously discussed, Horiguchi fails to disclose or teach, either expressly or inherently, an edge defined floating gate as required by each of Applicants' unamended independent claims 1, 7, and 14. Moreover, each of Applicants' amended independent claims 1, 7, and 14 require edge defined gates having sub lithographic dimensions, and Horiguchi fails to disclose or teach, either expressly or inherently, edge defined vertical gates having sub lithographic dimensions, since Horiguchi uses standard lithography for production of gates.

Further, Watanabe does not disclose or teach, either expressly or inherently, edge-defined floating gates as required by Applicants' unamended independent claims 1, 7, and 14. Additionally, Watanabe's gate dimensions are determined by lithographically defined geometrics. In fact, standard photo lithographic technique is used in Watanabe. (E.g., Watanabe, col. 2, lines 34-36; col. 9, lines 8-14; col. 11, lines 16-21 and 43-48) Correspondingly, sub lithographic gate dimensions are not achieved as is required by each of the Applicants' amended independent claims 1, 7, and 14.

As was previously asserted by the Applicants in response to the Examiner's First Office Action Rejection, Hong is directed to a top floating-gate flash EEPROM structure. Hong does not disclose or teach, either expressly of inherently, edge defined floating gates as required by each of the Applicants' unamended independent claims 1, 7, and 14. Moreover, Hong uses conventional lithography and does not achieve sub lithographic dimensions as is required by each of the Applicants' amended independent claims 1, 7, and 14. (E.g., Hong, col. 3, lines 52-54; col. 4, lines 29-34)

It is of course fundamental that in order to sustain an obviousness rejection, each and every required element must be shown to exist, either expressly or inherently in the cited references, standing alone or in combination. However, as presented above, none of the relied upon references standing alone or in combination, teach or disclose, either expressly or

inherently an edge defined floating gate, as is required by Applicants' unamended independent claims. Moreover, as presented above, none of the relied upon references standing alone or in combination, teach or disclose, either expressly or inherently, edge defined gates having sub lithographic dimensions, as is required by each of the Applicants' amended claims 1, 7, and 14. Accordingly, the Applicants respectfully request that the rejection of claims 1-23 be withdrawn.

Further, 2-6, 8-12, and 15-23, and 19-23 are dependent claims derived from the rejected independent claims 1, 7, and 14, respectively. Thus, the rejections of these claims are no longer sustainable, and the Applicants respectfully request that these rejections also be withdrawn.

CONCLUSION

Applicants sincerely believe that the above amendment and response represents a complete response to each and every rejection presented by the Examiner.

Furthermore, the Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Joseph Mehrle, at (612) 373-6975 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date 12/17/2001 By _____
Edward J. Brooks, III
Reg. No. 40,925

I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

_____
Tina M. Pugh

12/17/01
Date of Transmission